Ultra Low Current DC Characterization at the Wafer Level

Application Note 4070-1

Agilent 4072A Semiconductor Parametric Test System

Introduction

The continuing trend of smaller and smaller device geometries for the next generation of ULSI devices creates many new parametric testing challenges. In particular, the need for low current measurements in semiconductor process integration and process monitoring is becoming more and more critical.

The Agilent 4062UX Process Control System has been a well-accepted tool for both monitoring and developing semiconductor processes and is known for its ability to measure reliably low current down to the pA level.

Today, the Agilent 4072A performs low current measurements down to the 50 fA level, reliably and quickly. In order for the 4072A to perform such precise measurements, the appropriate fixturing, probe card and measurement techniques are required.

This application note describes the procedures required to precisely evaluate ultra-low current characteristics of a device under test (DUT) when using the 4072A.

Factors That Affect Low Current Measurement when using an Automatic Wafer Prober

This section discusses factors in the test environment that can negatively influence low current measurements.

Insulating Material

The need to use high-resistance insulation materials in prober interface components, such as the personality board, cables, probe card, and others, is essential to ensure the reliability of ultra-low current measurements. Poor insulation will allow greater leakage current.

Leakage on the Surface of the Prober Interface

Contaminants such as moisture or ionic chemicals can cause electrochemical effects that degrade insulation resistance. If the PC board used for the personality board or the probe card is ionically contaminated, a conductive path can be created and insulation resistance can be reduced. In some cases, ionic chemicals create a battery effect that sources offset current. This effect was once a major obstacle to obtaining reliable low-current measurements

Humidity and Temperature

As noted above, it is important to maintain constant low humidity in the test environment in order to prevent the occurrence of an electrochemical effect.

Likewise, keeping the temperature in the test environment constant is also important. Temperature changes can create contaminating condensation that, in turn, can lead to a serious degradation in the accuracy of low current measurements.

Light

Electron-hole pairs that are generated on the wafer by light can create currents which negatively impact low current measurements. Current caused by light is unstable and slow to change.

Cable Noise

Cable noise can be caused in two ways: by the triboelectric effect and by the piezoelectric effect. The triboelectric effect is the result of friction caused by motion at the boundary between the conductor and the insulator. The piezoelectric effect is the result of mechanical stress applied to the insulator.

Current from both of these effects can negatively influence low current measurements.

Outside Noise

Power line noise is one of the major sources that can negatively affect low current measurements. In general, automatic wafer probers require large amounts of power and, as a result, generate a significant amount of noise. In addition, the prober chuck, which has large surface area, can act as an antenna and absorb noise from outside the test environment.

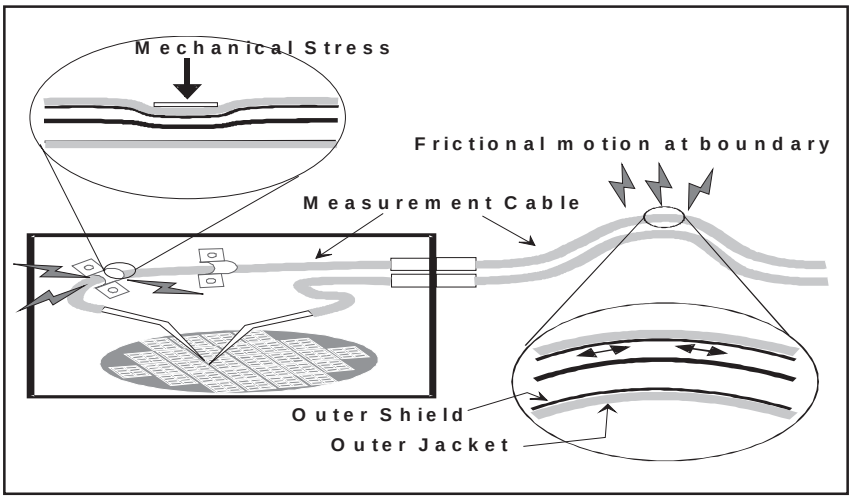


Figure 1. Piezoelectric and triboelectric effects.

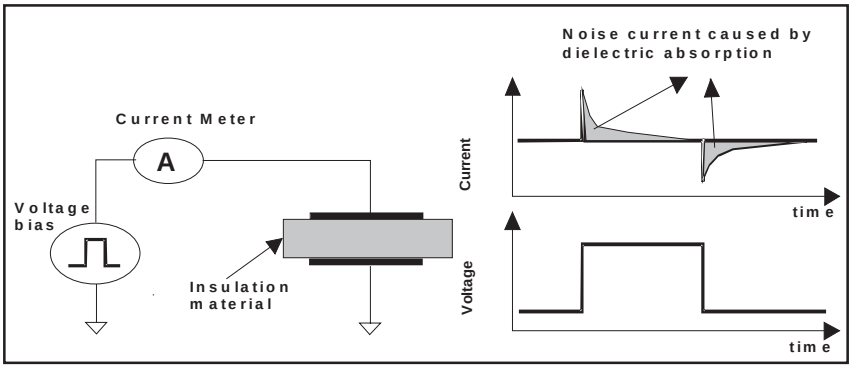


Figure 2. Dielectric absorption effect.

Dielectric Absorption

Dielectric absorption occurs when an electric field comes in contact with insulation. When applied voltage is changed, dielectric absorption can cause leakage current to flow (see Figure 2).

The amount of the current caused by dielectric absorption depends on the type of insulation and the strength of the electric field. This current will dissipate over time, thus rendering any compensation technique ineffective.

If dielectric absorption occurs, it is critical to wait until its effects have dissipated sufficiently so that the proper low current is measured, not the leakage current.

In the past, dielectric absorption has been a major problem when attempting to perform low current measurements quickly and accurately.

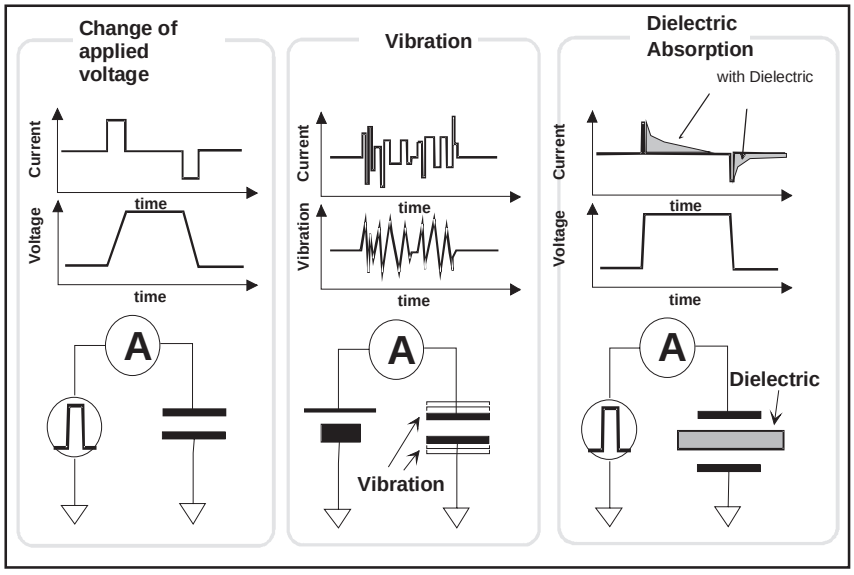


Figure 3. Capacitive coupling.

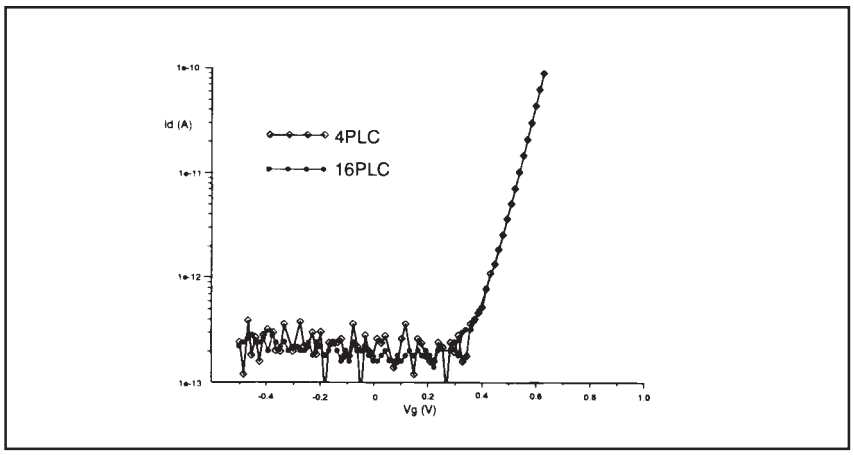


Figure 4. Id-Vg characteristics measured by the Agilent 4062UX.

Capacitive Coupling

Capacitive coupling is another bothersome source of noise current that occurs in two distinct ways: by a change in applied voltage, and by vibration.

$$I = C\frac{dV}{dt} + V\frac{dC}{dt}$$

For example, noise can be caused by a change in capacitance that results from vibration. There are also times when capacitance will exhibit current flow as the result of dielectric absorption. This can occur even if the insulation is not in contact with the conductor.

Offset

The ideal measurement instrument shows no current flow when nothing is connected to the DUT interface and no voltage is being applied. However, in a real-world test environment a measurement system will have a certain amount of offset current. This offset current will distort the value of the low current that is intended to be measured.

Leakage from Chuck Top to Ground

There are three main causes of current leakage from the chuck top to ground: contamination coating vacuum holes and tubes that run through the insulation that isolates the chuck from the Z-stage; insufficient guarding for the connection between the tester and the chuck top; and Z stage motor noise that is picked up by the chuck top.

The most recent prober designs have largely solved these problems.

Making Low Current Measurements with the Agilent 4072A

The Agilent 4062UX can reliably measure low current around 500 fA, with an integration time of 16 PLC (Power Line Cycles). To achieve its top performance level, however, the 4062UX must use a fully-guarded, blade-type probe card. (Figure 4 shows an example of Id-Vg characteristics as measured by the 4062UX).

The 4072A is able to make ultra-low current measurements of 50 fA in a real-world wafer test environment largely because of its built-in architectural features.

This section describes elements of the 4072A's architecture that allow it to make reliable, ultra-low current measurements. (Additional requirements affecting the 4072A's performance are discussed in the next section.)

Elements of the Agilent 4072A's Architecture that Allow Ultra-low Current Measurements

All of the factors described in the previous section need to be taken into consideration when making ultra-low current measurements with the 4072A. However, the system's architecture has built-in features that mitigate, and in some cases eliminate, negative effects that can compromise the reliability of the measurements.

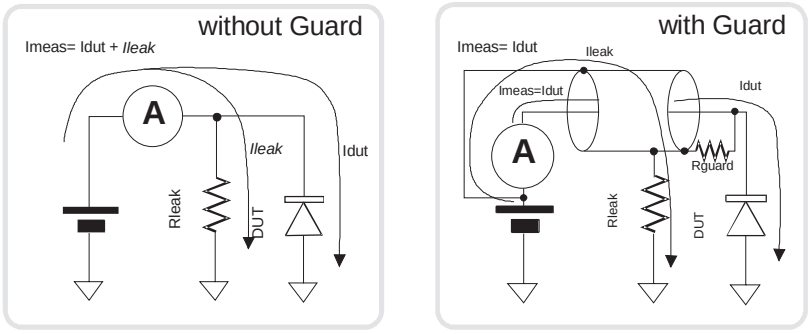
- The size of the 4072A's SMU is small enough to fit into the test head. The result is that noise generated at the cables between the test head and the system cabinet is eliminated.

- Heat generated in the test head is drawn out through the air duct. The temperature in the test head is, therefore, kept constant — eliminating the possibility of measurement fluctuation caused by a temperature shift.

- Two of the 4072A's eight ports are specially designed with fully guarded force lines. Full guarding of the force lines is the key to the system's ability to make reliable ultra- low current measurements (see Figure 5). When making low current measurements, it is important to select low current ports (see Figure 6).

- The direct docking mechanism (where the test head's output pins directly contact the probe card) reduces the parasitic factor — an effect normally caused by a conventional prober interface or bird cage. This feature of the 4072A's architecture eliminates the occurrence of dielectric absorption current and leakage current. In addition, the chance that moisture, body oil, or dust could contaminate the probe card interface is drastically reduced. This means that noise current caused by electrochemical effects at the prober interface is diminished.

- The high-precision AD Converter (ADC) used by the 4072A has a resolution of 10 fA that makes possible revolutionary improvements in resolution and accuracy when making low current measurements with an auto prober.



- Surround output force line with guard shield that has the same potential as the output terminal.
- Leakage current by Rleak doesn't affect measurement because the current doesn't flow through a meter.

Figure 5. Guarding technique.

```
FNPort(0,1)
FNPort(0,2)

Example)
 4500  Connect(FNPort(0,2), Gate)       ! Connect Low I port 2 to Gate
```

Figure 6. Specifiers for low current ports.

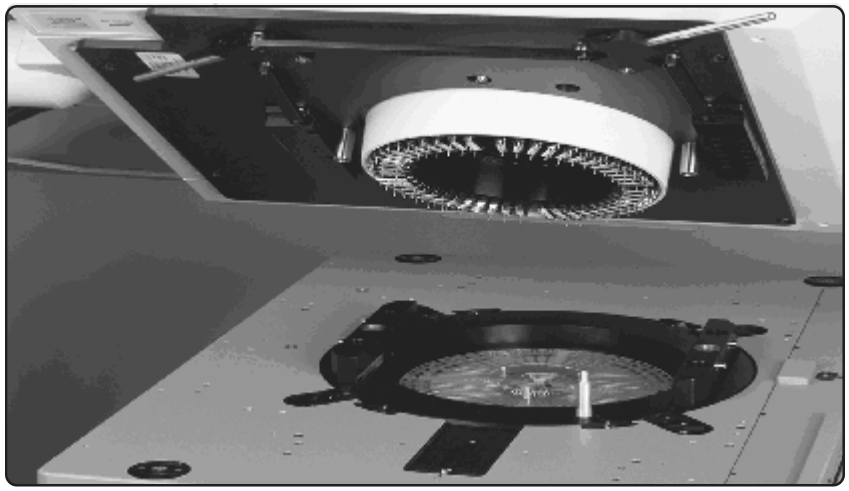


Figure 7. Direct docking.

Because it is an integration-type ADC, it functions as a low-path filter that effectively reduces high-frequency noise. In addi tion, if the integration time is set to equal a multiple of the AC power line cycle, the ADC can greatly reduce power line noise. Setting integration time is easily accomplished by using TIS (Test Instruction Set) commands (see Figure 8).

The 4072A is also equipped with a high-speed ADC that resides inside each SMU. In default mode, this type of ADC is used for making measurements. For making low current measurements, however, it is much more effective to use the high-precision ADC. In order to switch between the high-precision and high-speed ADCs, it is necessary to call the Set_smu_ch command (see Figure 8).

```
3200   Adc = 1                          ! High-speed: 0,   High-precision: 1
3210   Integ = 3                        ! Short : 1,  Med: 2, Long: 3, Manual: 0
3220   Plc = 32                         ! # of PLC ( 1 to 100 for Long)
3230  Set_smu_ch(FNPort(0,2), Adc)      ! Selecti High-precision ADC for port 2
3240  Set_adc(Adc, Integ, Plc)          ! Set integration time to 32 PLC
```

Figure 8. Example of code used to select the high-precision ADC and to specify integration time.

Additional Requirements for Making Reliable Ultra-low Current Measurements with the Agilent 4072A

Although the 4072A's architecture has many features that reduce or eliminate undesired phenomena (such as electrochemical contamination and dielectric absorption), other steps must be taken to enable the system to make ultra-low current measurements down to the 50 fA level. This section details those procedures.

Proper shielding must be used to block light sources that could generate electron-hole pairs on the wafer (see Figure 9).

The temperature of the test environment must be kept constant and the humidity low.

The prober interface must be kept free of contaminants such as dirt, moisture, and body oil. When changing the probe card, the use of clean gloves and a face mask can eliminate these problems. If the probe card or the prober interface become contaminated, they should be wiped with a lint-free cloth and 2-propanol.

Vibration resulting from movement in the test environment must be reduced as much as possible.

Choosing a properly designed and manufactured probe card is essential for obtaining maximum performance from the 4072A.

The probe card should be constructed of material that has a high isolation resistance and designed in a manner that reduces dielectric absorption. The material from which it is made should also be resistant to absorbing moisture, as this will also degrade performance.

The probe card's circuit pattern should be designed with a guard that fully covers the force line. This will reduce leakage current and dielectric absorption caused by parasitic effects (see Figure 10).

Figure 11 shows the results of an experiment to determine the amount of dielectric absorption current produced when using different probe cards and interfaces in an actual wafer probe test environment. In the experiment, 100 V was applied to the open pin to intentionally produce a large amount of dielectric absorption. The results show that a direct docking mechanism performs better than does a conventional bird cage interface. It is interesting to note that the difference in performance relates directly to the material from which the probe card is made and to its design pattern. Probe Card B is made of better PC board material than Probe Card A and has a superior circuit design.

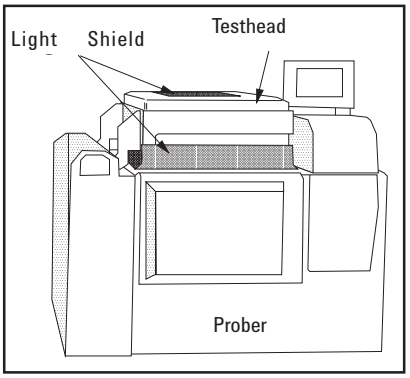


Figure 9. Example of light shielding.

If dielectric absorption current appears after applying high voltage, an appropriate amount of time must pass before a low current measurement is taken. This ensures that the dielectric absorption current has stabilized. To determine the proper waiting time, measure I-t characteristics by applying the same voltage as would be applied in an actual test. If a low voltage is applied, the amount of dielectric absorption current will be small and the time it takes to stabilize will be very short. When using the 4072A, the Wait_th command is used to specify the hold time after forcing the bias voltage. The Set_iv and Set-lsearch commands are also used with respect to specifying hold and delay time.

Figure 12 shows I-t characteristics when 0.1 V is applied to an open pin — no dielectric absorption is observed. In a real-world test application, where less than 10 V is applied, dielectric absorption will be negligible if a properly designed and manufactured probe card is used.

To obtain reliable low current measurements the appropriate integration time must be set (see Figure 8). The longer the integration time, the more accurate the measurement will be. Figure 13 shows Id-Vg characteristics measured with various integration times. The results indicate that an integration time of more than 3PLC is required to reliably measure at the 500 fA level, while an integration time of more than 16PLC is required to measure down to 50 fA.

Offset current generated by the test instrument must be subtracted from the total amount of low current measured.

To make ultra-low current measurements, not only should the force line on the probe card be guarded but, ideally, the probe blade and pins should also be fully guarded. Figures 14 and 15 show Id-Vg characteristics using probe cards with both guarded (coaxial) and unguarded (non-coaxial) pins. (The data in Figures 14 and 15 was obtained by setting the integration time to 1PLC and 16PLC respectively.) At an integration time of 1PLC, the difference in performance between coaxial and non-coaxial probe pins is significant, while at 16PLC the difference is small. When the applied voltage is high, there is a measurable differencein performance between coaxial and non-coaxial probe pins. However, in an actual test environment,

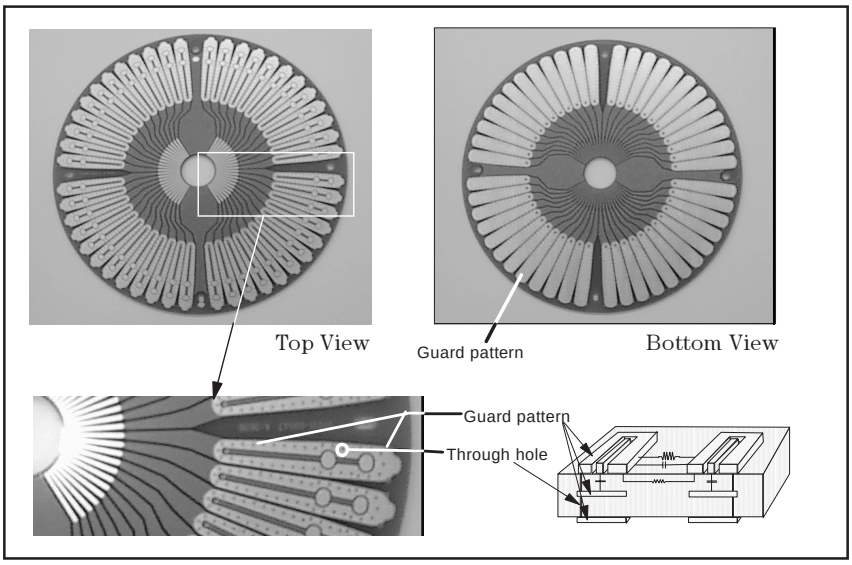


Figure 10. Example of fully guarded probe card.

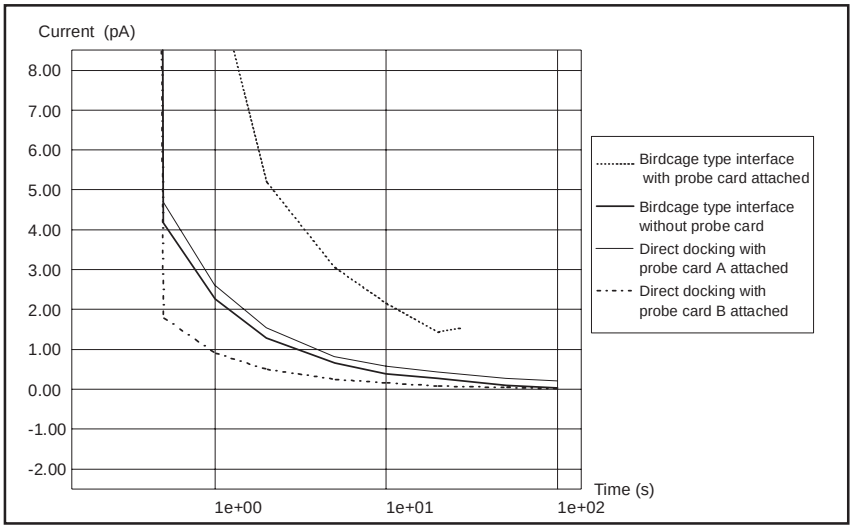


Figure 11. Dielectric absorption current observed when 100 V is applied (average of data taken at 6 pins).

where the applied voltage is not greater than 10 V, the difference is very small. This is especially true when the integration time is set to 16 PLC or greater.

Figure 16 on page 8 shows the relationship between standard deviation and integration time. In general, coaxial probe pins provide better repeatability than non-coaxial ones. However, at an integration time of 16PLC or greater, there is no difference between the two, and reliable low current measurements can be made down to the 50 fA level. This fact should be taken into consideration when choosing a probe card.

Because the prober chuck can act as an antenna and pick up noise from outside the test environment, proper guarding of the chuck will result in more accurate low current measurements.

Reliable ultra-low current measurements also require that

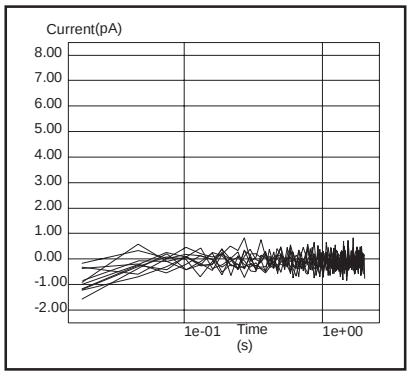


Figure 12. I-t characteristics when 0.1 V is applied (raw data at 10 different pins).

the design of the test structure be taken into account. If high voltage is applied to a terminal that is adjacent to a terminal used for measuring a differential voltage signal, leakage between the terminals will occur. In order to make ultra-low current measurements, the high voltage terminal should be separated from the other terminal and, if possible, should be guarded.

Conclusion

The Agilent 4072A can quickly perform reliable ultra-low current measurements down to the 50 fA level (see Figure 17 on page 8). However, an appropriate prober interface, probe card, and strictly controlled test environment are necessary for the system to reach its full potential.

Note The information in this application note also applies to the Agilent 4073A.

Contact your nearest Agilent sales office information about qualified probe card vendors.

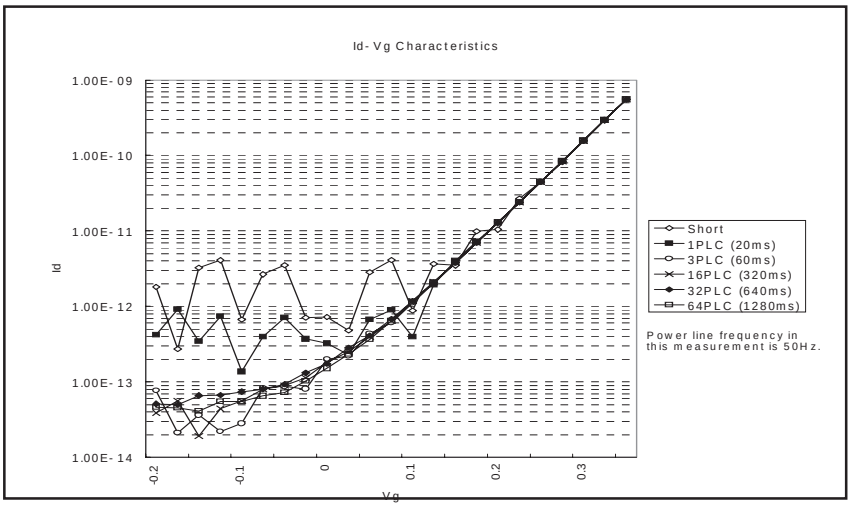


Figure 13. Id-Vg characteristics measured with various integration times.

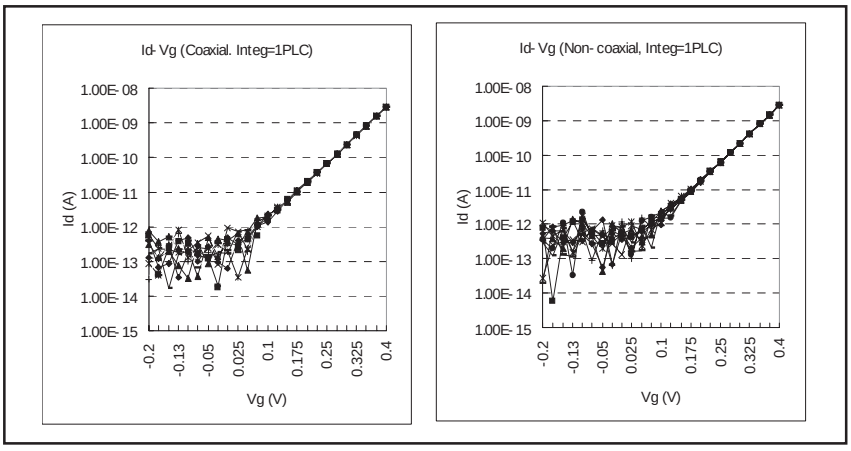


Figure 14. Id-Vg characteristics measured by using coaxial and non-coaxial probe pins (integration time = 1 PLC).

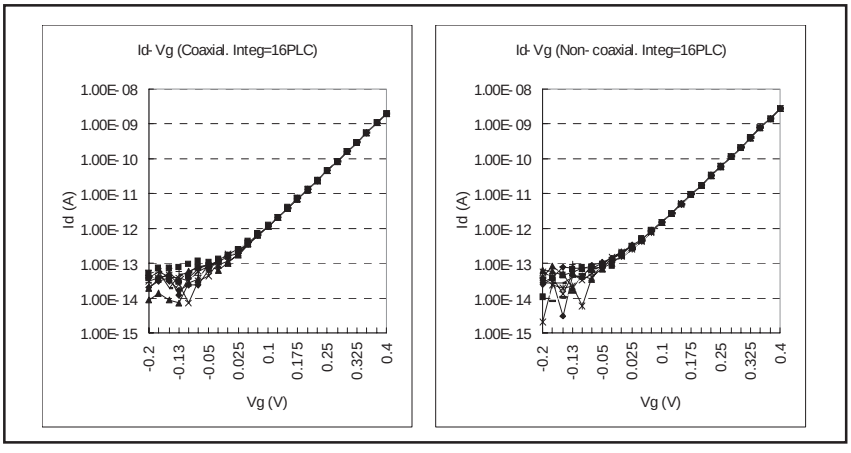


Figure 15. Id-Vg characteristics measured by using coaxial and non-coaxial probe card (integration time = 16 PLC).

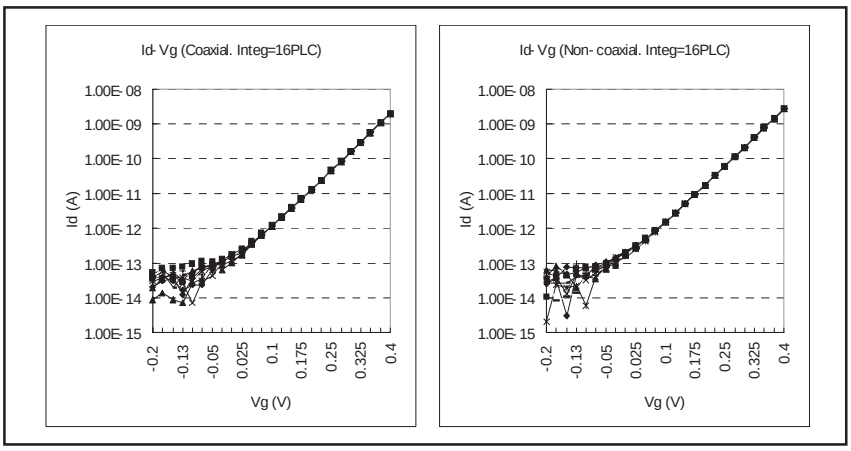


Figure 16. Repeatability difference between coaxial probe pin and non-coaxial probe pin.

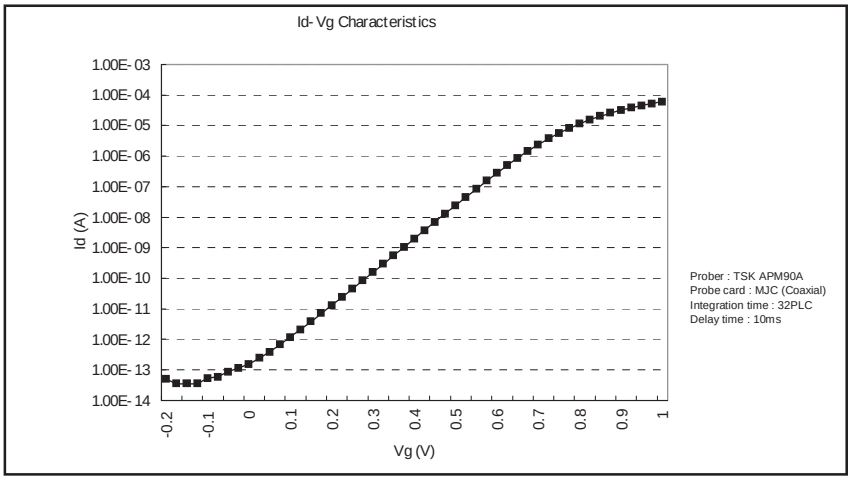


Figure 17. Id-Vg characteristics measured by the Agilent 4071A.

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